

METHOD AND APPARATUS FOR PHASE-SPLITTING A CLOCK SIGNAL

TECHNICAL FIELD

The invention relates to clocking circuits, and more particularly to circuits for generating a clock signal and a symmetrical complement of the clock signal. ✓

5 BACKGROUND OF THE INVENTION

Clock signals are commonly used in digital circuits, including circuits used in memory devices, to control the timing at which various events occur. In some cases, a single clock signal is used. However, in other cases, it is necessary to use both the clock signal and the complement of the clock signal. The signals are typically
 10 generated by applying a clock signal to a phase splitter, which then generates a clock signal and its complement for use by the digital circuit.

It is important that the clock signal and its complement be symmetrical, *i.e.*, the edges of both signals be substantially aligned and have the same slew rate. The clock signal and its complement generated by an ideal phase splitter would have a 50
 15 percent duty cycle, equal rise and fall times and they would be exactly 180 degrees out of phase from each other. In practice, the ideal is rarely achieved for a variety of reasons, including process variations in the fabrication of the phase splitter. For example, for a CMOS process, one pass of the process may result in an inverter having a fast NMOS transistor and a slow PMOS transistor, and another pass of process may
 20 result in the inverter having a slow NMOS transistor and a fast PMOS transistor. As a result, the inverters will respond differently to incoming clock signal, and the respective clock signals generated by the inverters will not be symmetrical.

A conventional phase splitter 10 is illustrated in Figure 1. The phase splitter 10 includes two branches 12, 14, one of which generates a signal OUT and the
 25 other which generates its complement OUT*. The second branch 14 consists of three inverters 20, 22, 24. Since there are an odd number of inverters in the second branch 14, the complementary output signal OUT* is the complement of the input signal CLK,

but delayed in time by the sum of the propagation delays through each of the inverters 20-24.

The first branch 12 consists of two inverters 30, 32 and a capacitor 34 connected to the output of the first inverter 30. The size of the capacitor 34 is selected to delay the coupling of all of signals from the output of the first inverter 30 to the input of the second inverter 32 by an amount corresponding to the difference between the delay of the three inverters 20-24 and the two inverters 30, 32. As a result, the OUT signal and the OUT* signal are theoretically 180 degrees out of phase with each other. In practice, however, the OUT and OUT* may not be entirely symmetrical for several reasons. For example, although the capacitor 34 compensates for the delay of the extra inverter in the second branch 14, it also reduces the slew rate of the signal applied to the input of the inverter 32. As a result, the slew rate of the signal applied to the inverter 32 is substantially slower than the slew rate of the signal applied to the inverter 24. This difference in slew rates causes the rise and fall times of the signals OUT and OUT* to differ substantially from each other.

Proposals have been made to modify the prior art phase splitter 10 shown in Figure 1 by dispensing with the capacitor 34 and instead adjusting the delay of each of the inverters 20-24, 30, 32 to achieve substantially the same result. More specifically, the inverters 20, 24 and 30 may be designed so that the sum of the delays through the inverters 20, 24 is equal to the delay through the inverter 30. The inverters 22 and 32 are then designed so that they have equal propagation delays. As a result, the signals OUT and OUT* are, in theory, symmetrical. Again, in practice, the signals are anything but symmetrical for several reasons. For example, the inverters 20, 24 must be relatively fast so that the sum of their delays is equal to the delay of the inverter 30. The high-speed of the inverter 24 causes it to have a relatively high slew rate. In order for the slew rate of the OUT signal to match the slew rate of the OUT* signal, the transistors used in the inverter 32 must be relatively large. However, the inverter 30 must be fairly slow to achieve the required delay, and, as a result, its output signal has a relatively low slew rate. The low slew rate of the inverter 30 makes it all the more difficult for the output of the inverter 32 to match the output of the inverter 24 so that

OUT and OUT* will have the same rise and fall times. If the slew rate of the inverter 24 is decreased to match the slew rate of the inverter 32, the speed of the inverter 32 will also be reduced. As a result, is necessary to increase the speed of the inverter 20 by a commensurate amount, thereby making the inverter 20 very large. In addition to
 5 consuming a relatively large area of the substrate, making the inverter 20 large decreases the input impedance of the inverter 20 making it difficult for other circuits (not shown) to drive the inverter 20.

A need therefore exists for a phase splitter that uses relatively little circuitry consuming relatively little area on a substrate that produces from a clock
 10 signal complementary signals that are substantially symmetrical in both phase and slew rate despite fabrication processing variations.

SUMMARY OF THE INVENTION

A phase splitter in accordance with the invention is operable to generate first and second complimentary output clock signals from an input clock signal. The
 15 phase splitter includes two branches receiving the input clock signal and generating the respective output clock signals. The first branch includes an even number of series connected inverters while the second branch includes an odd number of series connected inverters. In one aspect of the invention, an inverter is coupled between an output of an inverter in the first branch that is N number of inverters from the input
 20 clock signal and an output of an inverter in the second branch that is N+1 number of inverters from the input clock signal, where N is a positive integer, and where the added inverter's input is on the second branch and its output is on the first branch. Cross-coupling signals between the first and second branches in this manner provides delay but subsequently has increased the slew rate of the signal applied to an input of one of
 25 the inverters. In another aspect of the invention, a first pair of diode-connected transistors are coupled between an output of one of the inverters in the first branch that is M inverters from the input clock signal, and M + P inverters in either branch, to make the phase splitter substantially insensitive to process variations. M is a positive integer and P is positive even number. For the same reason, a second pair of diode-connected

transistors are coupled between an output of one of the inverters in the second branch that is M inverters from the input clock signal, and M + P inverters in either branch.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a logic diagram of a conventional phase splitter.

5 Figure 2 is a logic diagram of a phase splitter according to one embodiment of the invention.

Figure 3 is a logic diagram of a phase splitter according to another embodiment of the invention that is similar to the embodiment of Figure 2.

10 Figure 4 is a logic diagram of a phase splitter according to another embodiment of the invention.

Figure 5 is a logic diagram of a phase splitter according to another embodiment of the invention that is similar to the embodiment of Figure 4.

Figure 6 is a logic diagram of phase splitters according to another embodiment of the invention.

15 Figure 7 is a logic diagram of phase splitters according to still another embodiment of the invention.

Figure 8 is a logic diagram of phase splitters according to another embodiment of the invention that is based on a modifications of the phase splitters of Figures 2-7.

20 Figure 9 is a block diagram of an embodiment of a synchronous dynamic random access memory that uses one or more of the phase splitters shown in Figures 2-8.

Figure 10 is a block diagram of an embodiment of a computer system using the SDRAM of Figure 9.

25 DETAILED DESCRIPTION OF THE INVENTION

A phase splitter 40 in accordance with one embodiment of the invention is illustrated in Figure 2. Like the prior art phase splitter 10 shown in Figure 1, the phase splitter 40 includes two branches 42, 44 that generate OUT and OUT* signals,

respectively. The first branch 42 includes two inverters 46, 48, while the second branch 44 includes three inverters 50, 52, 54. The phase splitter 40 differs from the prior art phase splitter 12 shown in Figure 1 in two primary respects. First, it includes an inverter 60 coupled from the output of the inverter 52 to the input of the inverter 48.

Second, the phase splitter 40 includes first and second pairs 64, 66 of diode-coupled transistors coupled from the output of the inverter 54 to the input of the inverter 48 and the input of the inverter 52, respectively. Each transistor pair 64, 66 includes an NMOS transistor 70 with its “anode” coupled to the output of the inverter 54 and a PMOS transistor 72 with its “cathode” coupled to the output of the inverter 54.

In operation, assume that the input signal IN is low. As a result, the output of the inverter 46 will be high and the output of the inverter 48 will be low. The outputs of the inverters 50 and 54 will also be high, and the output of the inverter 52 will be low, thereby causing the inverter 60 to output a high. Note that, in this condition, the circuit is in equilibrium because the OUT*, which is high, is coupled to the high outputs of the inverters 46, 50. Also, the high output of the inverter 60 is coupled to the high output of the inverter 46.

When the IN signal transitions high, the output of the inverter 46 attempts to transition low. However, this high-to-low transition is resisted by the high at the output of the inverter 54, which is coupled through the NMOS transistor 70 in the transistor pair 64. As a result, there is a delay before the transition voltage of the inverter 48 is reached. The magnitude of the delay can be adjusted by adjusting the ON impedance of the NMOS transistor 70 in relation to the impedance of an NMOS transistor (not shown) in the inverter 46. In a similar manner, the output of the inverter 50 attempts to transition low, but is resisted by the high coupled from the OUT* terminal to the input of the inverter 52 through the NMOS transistor 70 in the transistor pair 66. Both transistors 70 of pair 64 and 66 are tuned such that the delays of both branches 40 and 44 match each other over various process and operating conditions. This is not to say that the delays are constant between different processes, but that both branches track each other. Also, each transistor 70 not only compensates the NMOS transistors in inverters 46 and 50 (not shown), but also compensates their respective

entire branch. Eventually, the outputs of the inverters 48, 52 transition high, and the output of the inverter 54 transitions low. When the output of the inverter 54 transitions low, the power drain through the transistors 70 in the transistor pairs 64, 66 is eliminated.

5 When the IN signal transitions low, the outputs of the inverters 46, 50 attempt to transition high, but are held low through the PMOS transistors 72 in the transistor pairs 64, 66, respectively. Again, the magnitude of the resulting delay can be adjusted by adjusting the ON impedance of the PMOS transistors 72 in the transistor pairs 64, 66 in relation to the impedance of a PMOS transistors (not shown) in the
10 inverters 46, 50 respectively. Again, the PMOS transistors 70 are tuned to match the branches. When the outputs of the inverters 48, 52 transition low and the output of the inverter 54 transitions high, the power drain through the transistors 72 in the transistor pairs 64, 66 is eliminated.

 The characteristics of the transistor pair 64 are thus preferably set so that
15 the transistor pair 64 counteract for process variations in both of the inverters 46, 48. Similarly, the characteristics of the transistor pair 66 are preferably set so that the transistor pair 66 counteracts process variations in all three of the inverters 50, 52, 54, thereby maintaining the symmetry of the OUT and OUT* signals.

 If power drain is not a factor, the phase splitter embodiment 40' shown
20 in Figure 3 may be used. The phase splitter 40' of Figure 3 uses the same components as the phase splitter 40 of Figure 2, and its components have therefore been provided with the same reference numerals. In the phase splitter 40' of Figure 3, the drains of the NMOS transistors 70 in the transistor pairs 64, 66 are coupled directly to a supply voltage V_{CC} instead of to the output of the inverter 54. As a result, the NMOS
25 transistors 70 continuously bias the outputs of the inverters 46, 50 high to delay the high-to-low transitions at the outputs of the inverters 46, 50. Since both transistors 70 are tuned so that the delays of the branches 40 and 44 match each other over various process and operating conditions, each transistor 70 not only compensates the NMOS transistors in inverters 46 and 50 (not shown), but also compensates their respective
30 branches.

The phase splitter 40' of Figure 3 also differs from the phase splitter 40 of Figure 2 by the coupling the drains of the PMOS transistors 72 to ground instead of to the output of the inverter 54. Again, the PMOS transistors 72 continuously bias the outputs of the inverters 46, 50 low to delay the low-to-high transitions at the outputs of the inverters 46, 50, thereby compensating the PMOS transistors in inverters 46 and 50 and compensating for process variations in their respective branches.

As mentioned above when describing the prior art phase splitter 12 of Figure 1, the speed of the inverter 46 will generally be relatively slow compared to the speed of the inverters 50, 54. As a result, the signal at the output of the inverter 46 would have a relatively slow slew rate, thereby necessitating the inverter 48 be relatively large to produce an OUT signal having a sufficiently fast slew rate. However, in the embodiment of a phase splitter 40 shown in Figure 2, the presence of the inverter 60 allows the inverter 48 to be relatively small and still produce an OUT signal having a relatively fast slew rate. This is accomplished by using the output of the inverter 60 to assist each transition at the output of the inverter 46. More specifically, when the IN signal transitions high, the output of the inverter 46 transitions low and the output of the inverter 52 subsequently transitions high. As a result, after a short delay, the output of the inverter 60 transitions low to complement the low output of the inverter 46. Thus, in response to the IN signal transitioning high, the output of the inverter 46 initially transitions low with a relatively slow slew rate. After a short delay, the high-to-low transition at the output of the inverter 60 substantially increases the slew rate. In this is faster slew rate to which the inverter 48 responds thereby producing the OUT signal with a sufficiently fast slew rate. The embodiment of the phase splitter 40 illustrated in Figure 2 is thus substantially insensitive to process variations and is able to provide symmetrical OUT and OUT* signals without the use of large transistors.

An alternative embodiment of a phase splitter 80 is shown in Figure 4. The phase splitter 80 includes many of the components that are used in the phase splitter 40 of Figure 2. Therefore, in the interest of brevity, an explanation of these components will not be repeated. The phase splitter 80 includes two additional inverters 84, 86. The transistor pair 72 remains coupled to the output of the inverter 54.

However, the transistor pair 64 is now coupled to the output of the inverter 86, which generates the OUT* signal. Since each inverter 54, 86 drives only a single transistor pair 64 or 66, the transistors in the inverters 54, 86 may be smaller than the transistors in the inverter 54 used in the phase splitter 40 of Figure 2. Alternatively, the inverters 54, 86 may be the same size, but the size of the transistors 70, 72 in each transistor pair 64, 66 can be smaller because each inverter 54, 86 is loaded by only a single transistor pair 64, 66.

As with the phase splitter 40' of Figure 3, the embodiment of Figure 5 may be used if power drain is not a factor. The phase splitter 80' of Figure 5 differs from the phase splitter 80 of Figure 4 in the same manner that the phase splitter 40' of Figure 3 differs from the phase splitter 40 of Figure 2. Specifically, the drains of the NMOS transistors 70 in the transistor pairs 64, 66 are coupled directly to a supply voltage V_{CC} instead of to the output of the inverter 54, and the drains of the PMOS transistors 72 are coupled directly to ground instead of to the output of the inverter 54. As explained above with reference to Figure 3, the NMOS transistors 70 and the PMOS transistors 72 continue to compensate the transistors in inverters 46 and 50 and their respective branches.

Another embodiment of a phase splitter 100 is shown in Figure 6. This embodiment also uses the same components as the phase splitter 40 of Figure 2, and its components have therefore been provided with the same reference numerals. The phase splitter 100 of Figure 6, operates in much the same way as the phase splitter 40 of Figure 3. However, the drains of the NMOS transistors 70 are coupled to the supply voltage V_{CC} , and the drains of the PMOS transistors 72 are coupled to ground. These topographical changes alter the operation in two respects. First, the transistors 70, 72 no longer operate as diodes. Second, the current is supplied to the outputs of the input inverters 46, 50 from either V_{CC} or ground rather than by the inverter 54. As a result of the reduced current demand, the inverter 54 may be made sufficiently smaller.

In operation, the NMOS transistors 70 initially bias the outputs of the inverters 46, 50 high to delay the high-to-low transitions at the outputs of the inverters 46, 50. When the output of the inverter 54 has transitioned low, the NMOS transistors

70 are turned OFF to conserve power. Similarly, the PMOS transistors 72 initially bias the outputs of the inverters 46, 50 low to delay the low-to-high transitions at the outputs of the inverters 46, 50. When the output of the inverter 54 has transitioned high, the PMOS transistors 72 are turned OFF to conserve power.

5 Still another embodiment of a phase splitter 102 is shown in Figure 7. The topography of this embodiment is identical to the phase splitter 100 of Figure 6 except that the drains of the NMOS transistors 70 are coupled to ground through an NMOS transistor 92, and the drains of the PMOS transistors 72 are coupled to V_{CC} through a PMOS transistor 94. The ON resistance of the transistors 92, 94 provide
10 electro-static discharge ("ESD") protection. In all other respects, the phase splitter 102 operates in the same manner as the phase splitter 100 of Figure 6. The phase splitter 102 of Figure 6 can also be provides with inherent ESD protection by increasing the gate to contact spacing for the transistors 70, 72 on the drain side.

Although several specific examples of phase splitters according to the
15 invention have been provided, it will be understood that a wide variety of other circuit topographies may be used. For example, one or both of the diode-coupled transistors 70, 72 may be reversed so that the gates of the transistors 70, 72 in the transistor pairs 64 are coupled to the output of the inverter 46, and the gates of the transistors 70, 72 in the transistor pair 66 are coupled to the output of the inverter 50. Additionally, the
20 inverter 60 may be used without the transistor pairs 64, 66 to increase the slew rate of the signal applied to the inverter 48, and the transistor pairs 64, 66 may be used without the inverter 60 to compensate for process variations in the inverters 30, 32, 50-54.

In the field of semiconductors, it is common to scale up or down the size of components in circuits depending upon the load to be driven by the circuit. Thus, the
25 inverters used in the phase splitters 40, 40', 80, 80', 100, 102. However, as also understood in the art, there is a limit to how small semiconductor components can be scaled. Thus, when the phase splitters 40, 40', 80, 80', 100, 102 are scaled to their minimum size, the relative size of the inverters can change. In particular, the output inverters 48, 54 can continue to be scaled downwardly beyond the point that the input
30 inverters 46, 50 can no longer be scaled down. When scaling semiconductor circuits in

this manner, it is desirable for the timing relationships in the circuit to be insensitive to the scaling. However, when the ratio of the scaling of the output inverters 48, 54 to the scaling of the input inverters 46, 50 changes because the input inverters 46, 50 have reached their minimum sizes, the timing relationships in the phase splitter change. The timing relationship changes because the input inverters 46, 50 have been made larger relative to the size of the output inverters 48, 54, and are thus more easily able to drive the output inverters 46, 50. The signal from the output inverters 46, 50 thus transitions earlier relative to the transition of a clock signal applied to the input of the input inverters 46, 50. As a result, the scaling of the phase splitter alters the timing of the phase splitter.

The timing relationships in the phase splitters 40-102 can be made insensitive to the scaling of the phase splitters as shown in Figure 8, which shows pertinent portions of the phase splitters of Figure 2-7. An inverter 90 is coupled to the output of each input inverter 46, 50 to increase the load that is driven by the input inverters 46, 50. The inverters 90 are sized independently, if necessary, so that the switching times of the inverters 46-54 remain constant as the output inverters 48, 52 are scaled downwardly beyond the point where the input inverters 46, 50 can be scaled further. Since the inverters 90 are used only for loading the input inverters 46, 50, the outputs of the inverters 90 may be left unconnected to any other circuitry. However, if it is desired to couple the outputs of the inverters 90 to other circuitry, the inverters 90 can be used for this purpose. Although inverters 90 are used to load the inverters 46, 50 in the embodiment of Figure 8, it will be understood that other components, such as capacitors, can be used for that purpose.

The phase splitters 40-102 may be used in a variety of devices, including, as shown in Figure 9, a synchronous dynamic random access memory 110 ("SDRAM"). The SDRAM 110 includes a control logic circuit 114, an address decoder 116, and a read/write circuit 118, all of which are coupled to a memory array 120. As is well known in the art, the address decoder 116 receives an address over an address bus 22 and provides a decoded address to the memory array 120 to select an individual memory cell in the memory array. The read/write circuit 118 operates to receive data

over a data bus 124 and provide that data to the memory array 120 during a write operation, and to provide data from the memory array to the data bus during a read operation.

The SDRAM 110 performs data transfer operations under control of the control logic circuit 114 which receives data transfer commands, including read or write commands, over a control bus 126. In response to these data transfer commands, the control logic circuit 114 executes each of the steps required to perform a read or write data transfer operation. The SDRAM 110 also receives a CLK to control the timing of various operations. The CLK signal is converted to complimentary clock signals CLK-OUT and CLK-OUT* by one of the phase splitters 40, 80 or some other embodiment of a phase splitter (not shown) according to the invention. These CLK-OUT and CLK-OUT* signals are applied to the control logic circuit 114 to cause the control logic circuit 114 to synchronously execute one or more memory operations twice for each cycle of the CLK signal. These operations are performed at intervals that are spaced substantially equally from each other because of the symmetry of the CLK-OUT and CLK-OUT* signals provided by the phase splitter 40 or 80. A clock enable signal CKE enables the clocking of the control logic circuit 114 by the CLK-OUT and CLK-OUT* signals.

Figure 10 shows a computer system 200 containing the SDRAM 110 of Figure 9 using one of the phase splitters 40-102 or some other embodiment of a phase splitter (not shown) according to the invention. The computer system 200 includes a processor 202 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 202 includes a processor bus 204 that normally includes an address bus, a control bus, and a data bus. In addition, the computer system 200 includes one or more input devices 214, such as a keyboard or a mouse, coupled to the processor 202 to allow an operator to interface with the computer system 200. Typically, the computer system 200 also includes one or more output devices 216 coupled to the processor 202, such output devices typically being a printer or a video terminal. One or more data storage devices 218 are also typically coupled to the processor 202 to allow the processor 202 to store data in or

retrieve data from internal or external storage media (not shown). Examples of typical storage devices 218 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs). The processor 202 is also typically coupled to cache memory 226, which is usually static random access memory ("SRAM") and to the

5 SDRAM 110 through a memory controller 230. The memory controller 230 normally includes a control bus 236 and an address bus 238 that are coupled to the SDRAM 110. A data bus 240 may be coupled to the processor bus 204 either directly (as shown), through the memory controller 230, or by some other means.

From the foregoing it will be appreciated that, although specific

10 embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193